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PARK, JUNG H

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/658,216	SWENSON ET AL.	
	Examiner	Art Unit	
	JUNG PARK	2419	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21,24-46 and 49-88* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21,24-46,49-84 and 88* is/are rejected.

7)☒ Claim(s) *85-87* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Remark

1. This communication is considered fully responsive to the amendment filed on 12/22/08.

a. The Examiner acknowledges that all of the independent claims 1, 24, 53, 59, 65, 73, 81, and 83 have been amended.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-19, 21, 24-44, 46, 49, 50, 81, 83, and 88 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shankar et al. (US 2004/0066781, "Shankar") in view of Ryals et al. (US 6788671, "Ryals").

Regarding claim 1, Shankar discloses a system for communicating control information over one or more backplane connections between two or more entities comprising:

- first logic (a logic, not shown, to process VLAN ID within MAC controller, see ¶.43) for storing proprietary control information (storing unit and tables for saving control information within packets, see fig.4 and 500 & 510 fig.5), comprising control information recognized by the network entity but not recognized by other network entities (VLAN ID tags are used for identifying a unique VPLS customer via one of subscriber ports within a PE device, see ¶.41 and ¶.46; each outgoing bit map can correspond to a particular

port within the PE device, see ¶.52; VPLS port bit map can correspond to a particular port within the PE device, see fig.4 and ¶.50), within a layer of a packet above the physical layer (layer 2 packets, see fig.4-5); and

- second logic (a logic, not shown, to transfer the packet, see ¶.43 and fig.1-2) for communicating the packet, including the proprietary control information, over one or more of the connections (as shown in fig.1-2),

- wherein the proprietary control information (note: control information within packet shown in fig.5) as stored in the packet either replaces or appears in the packet to third party devices that may happen to gain access (appending and forwarding to other entities, see 725 & 730 fig.7; 830 & 835 fig.8; 925 & 930 fig.9; 1045 & 1050 fig.10) as at least a portion of one or more standard packet fields (a portion of packet fields, see fig.5);

- wherein the first logic derives at least a portion of the control information from a packet header (identify VLAN ID, see 905 fig.9), and deletes the packet header prior to communication of the packet over the one or more backplane connections (removing, see 915 fig.9), and wherein a third logic for re-creating at least a portion of the packet header from the control information after communication of the packet over the one or more backplane connections (replacing, see 925 and 930 fig.9).

Shankar does not explicitly disclose the limitations of “a backplane and wherein the deviations, deletions, and recreations of the packet header mitigate bandwidth limitations caused by the backplane connections and improve system throughput.” However, Ryals discloses "a backplane (428 fig.4 and col.7, ln.1)” which is a common backplane for transporting information between the various interface cards (see 108 fig.1 and col.1, ln.28-35) that connects the cards to each other to make up a complete a

computer system. Ryals, further, discloses "wherein the deviations, deletions, and recreations of the packet header mitigate bandwidth limitations caused by the backplane connections and improve system throughput (by reducing the messaging traffic over backplane the throughput of switching device is increased, see col.3, ln.30-33)." Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use a common backplane disclosed by Ryals into the system of Shankar in order to support the maximum transfer rate of the backplane. The motivation of using backplane is to insert some interface cards into the backplane because of its convenient to install and replace, and also reliability of the backplane system. Further, the deviation, deletions, and recreations of the packet header are for reducing the message traffic over backplane connections so that the throughput of switching device is increased as disclosed by Ryals (see col.3, ln.30-33).

Regarding claim 2, Shankar discloses, "wherein the control information is stored in at least a portion of one or more fields inserted into the packet by the first logic (store to determine if the incoming packet is addressed to a particular port, see ¶.42)."

Regarding claim 3, Shankar discloses, "wherein the first logic overwrites at least a portion of one or more pre-existing fields in the packet with the control information (source address can be supplied by the transmitting MAC, see ¶.43)."

Regarding claim 4, Shankar discloses, "wherein the two or more entities comprise a switch (fig.3), and the control information is proprietary to the switch (fig.5a-

b)."

Regarding claim 5, Shankar discloses, "wherein the switch has ingress and egress ports (ports in fig.2)."

Regarding claim 6, Shankar discloses, "wherein the proprietary control information comprises an identifier of an ingress port of the switch at which the packet was received over a network (VLAN ID, see fig.6)."

Regarding claim 7, Shankar discloses, "wherein the proprietary control information comprises an identifier of an egress port of the switch at which the packet will or is expected to be transmitted over a network (egress port for transmitting, see ¶.33; VLAN IDs for ports, see ¶.34 and fig.5)."

Regarding claim 8, Shankar discloses, "wherein the proprietary control information comprises an indicator of whether or not one or more predetermined fields were present in the packet upon receipt thereof at the switch (fig.5 and ¶.34)."

Regarding claim 9, Shankar discloses, "wherein the one or more predetermined fields comprise a VLAN (¶.34)."

Regarding claim 10, Shankar discloses, "wherein the control information is stored in layer two or higher of the packet according to the OSI reference model (layer 2, see fig.5 and ¶.62)."

Regarding claim 11, Shankar discloses, “wherein the control information is stored in layer two of the packet according to the OSI reference model (layer 2, see fig.5 and ¶.62).”

Regarding claim 12, Shankar discloses, “wherein the control information is stored in the MAC sub-layer of the packet (MAC, see ¶.43).”

Regarding claim 13, Shankar discloses, “wherein the control information overwrites at least a portion of a VLAN stored in the MAC sub-layer of the packet (¶.42 and ¶.43).”

Regarding claim 14, Shankar discloses, “wherein the control information overwrites at least a portion of source or destination addresses stored in the MAC sub-layer of the packet (SA and DA, see ¶.42).”

Regarding claim 15, Shankar discloses, “wherein the VLAN comprises op code and tag portions, and the first logic overwrites the op code portion of the VLAN with the control information (op-code and tag, see fig.5 and ¶.44).”

Regarding claim 16, Shankar discloses, “wherein the control information comprises an identifier of the VLAN op code overwritten by the control information (op-code modified, see ¶.76).”

Regarding claim 17, Shankar discloses, “wherein the VLAN is the outer VLAN of a plurality of nested VLANs (fig.1).”

Regarding claim 18, Shankar discloses, “wherein the control information comprises quality of service information for the packet (priority, fig.5 and ¶.67).”

Regarding claim 19, Shankar discloses, “wherein the quality of service information comprises an identifier of a queue for buffering the packet (buffer …identifying, see ¶.11) and priority for the queue is selected based on the QoS information of the packet (buffer with the priority tag, see ¶.11-12).

Regarding claim 21, Shankar discloses, “wherein by dropping a portion of the packet (915 fig.9), the control information is added to the packet and the packet is communicated in-band over the one or more backplane connections without requiring additional clock cycle (925 fig.9).”

Regarding claim 24, it is a claim corresponding to claim 1 and is therefore rejected for the similar reasons set forth in the rejection of claim 1.

Regarding claims 25-32, they are claims corresponding to claims 2-9, respectively and are therefore rejected for the similar reasons set forth in the rejection of the claims.

Regarding claim 33, Shankar discloses, "wherein the proprietary control information comprises an indicator of a state of the ingress port of the switch at which the packet was received (identifying …, see ¶.11)."

Regarding claims 34-38, they are claims corresponding to claims 10-13 and 9, respectively and are therefore rejected for the similar reasons set forth in the rejection of the claims.

Regarding claim 39, Shankar discloses, "one or more fields comprise source or destination addresses (fig.5)."

Regarding claims 40-44 and 46, they are claims corresponding to claims 15-19 & 21, respectively and are therefore rejected for the similar reasons set forth in the rejection of the claims.

Regarding claims 49 and 50, they are claims corresponding to claim 6 and are therefore rejected for the similar reasons set forth in the rejection of claim 6.

Regarding claim 81, it is a claim corresponding to the mapping step in claim 53 and the storing and communication steps in claim 1 and is therefore rejected for the similar reasons set forth in the rejection of claims 1 and 53.

Regarding claim 83, it is a claim corresponding to claim 81 and is therefore rejected for the similar reasons set forth in the rejection of claim 81.

Regarding claim 88, Shankar discloses, “a fourth logic that masks the control information such that the control information appears as a standard packet field to a third party (¶.46).”

4. Claims 20 and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shankar in view of Ryals and further in view of Kalkunte et al. (US 2002/0012345, “Kalkunte”).

Regarding claims 20 and 45, Shankar and Ryals lack what Kalkunte discloses, “wherein the control information comprises an indicator that the packet is a candidate for dropping (drop, see ¶.113).” Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention to apply the method of drop packets taught by Kalkunte into the forwarding method of Shankar and Ryals in order to maximize/optimize memory utilization based on ports.

5. Claims 51 and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shankar in view of Ryals and further in view of Williams (US 7031325, “Williams”).

Regarding claims 51 and 52, Shankar lacks what Williams discloses, “third logic (MAC logic, see 780 fig.7) for maintaining a mode bit (op-code, see 780 fig.7) having first and second states (insert or modify, see 780 fig.7), wherein the first logic is configured to add one or more fields to the packet layer to accommodate the control information (insert VLAN tag, see 780 fig.7 and col.12, ln.2-12) if the mode bit is in the first state (without the VLAN tag, see 780 fig.7), and overwrite at least a portion of one or more pre-existing fields in the packet layer (modified, 780 fig.7) with the control information if

the mode bit is in the second state (state for modifying, see 780 fig.7).” Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention to apply the op-code examining method taught by Williams into the VLAN tagging engine disclosed by Shankar in order for the engine to operate in accordance with multiple protocols.

6. Claims 53-64 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shankar in view of Ryals and further in view of Bare (US 2003/0142685, “Bare”).

Regarding claim 53, Shankar discloses a system for performing load balancing over a plurality of backplane connections between two or more entities, the system comprising:

- first logic (a logic, not shown, to process VLAN ID within MAC controller, see ¶.43) for receiving a packet at a first entity (600 fig.6), mapping control information (identifying VLAN ID, see ¶.43) for the packet into one or more identifiers (identifiers in the packets, see fig.5) of at least one of the one or more of connections coupling the first entity to a second entity (PE 1-n, see fig.1), the first and second entities comprising a network entity (see fig.1-2), wherein the mapping occurs through a data structure (look-up table, see 610 fig.6); and

- second logic for communicating the packet (a logic, not shown, to transfer the packet, see ¶.43 and fig.1-2) over the at least one of the one or more connections identified one or more identifiers (VLAN tags, see fig.5);

- wherein quality of service information is used to identify a queue into which the packet is stored (priority, see ¶.7, ¶.11-12 and 434 fig.4) before transmission over the one or more backplane connections (before forwarding to other module, see 730

fig.7and ¶.7) and priority for the queue is selected based on the QoS information of the packet (assigning priority based on CoS, see 715 fig.7 and ¶.7)

Shankar does not explicitly disclose the limitation of "backplane connections", which was rejected in claim 1. Therefore, this claim is rejected for the same reasons and motivation set forth in the rejection of claim 1.

Shankar lacks what Bare discloses, "to achieve a desired a desired load balancing of packets over the plurality of backplane connections (load balancing, see ¶.28 and ¶.383)." Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention to apply the load balancing protocols taught by Bare into the tagging engine of Shankar in order to optimize the utilization of available throughput in the network of switches.

Regarding claim 54, it is a claim corresponding to claims 4, 6, and 7 and is therefore rejected for the similar reasons set forth in the rejection of claims 4, 6, and 7.

Regarding claim 55, Shankar discloses, "wherein the first logic comprises a LUT (look-up tables, see fig.4) for maintaining an association between ingress or egress ports (fig.4 and ¶.41), and egress ports associated with the backplane connections (ports, see fig.4 and ¶.41), and the first logic maps a particular ingress or egress ports into one or more backplane-associated egress ports through an access to the LUT (relationship of ports and tables, see ¶.50 and ¶.52)."

Regarding claim 56, Shankar discloses, "wherein the association is programmed into the LUT (¶.50 and ¶.52)."

Regarding claim 57, Shankar lacks what Bare discloses, “wherein the association is pre-determined to achieve a desired load balancing of packets over the plurality of backplane connections (load balancing, see ¶.28 and ¶.383).” Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention to apply the load balancing protocols taught by Bare into the tagging engine of Shankar in order to optimize the utilization of available throughput in the network of switches.

Regarding claim 58, Shankar does not explicitly disclose, “wherein the two or more entities are each ASICs.” ASIC is a chip that is custom designed for a specific application rather than a general-purpose chip such as a microprocessor. Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use ASIC within PE of Shankar in order to improve performance over general-purpose CPUs, because ASICs are "hardwired" to do a specific job and do not incur the overhead of fetching and interpreting stored instructions.

Regarding claim 59, it is a claim corresponding to claim 53 and is therefore rejected for the similar reasons set forth in the rejection of claim 53.

Regarding claims 60-64, they are claims corresponding to claims 54-58, respectively and are therefore rejected for the similar reasons set forth in the rejection of the claims.

7. Claims 65-80, 82, and 84 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shankar in view of Ryals and further in view of Lou et al. (US 7173935, “Lou”).

Regarding claim 65, it is a claim corresponding to claim 1, except the limitations of “a first switch coupled to a second switch and the first switch having a greater number of n ports than the number of ports m of the second switch” and “wherein the second switch appears to the network to have n ports rather than m ports." However, Lou discloses, “a first switch coupled to a second switch and the first switch having a greater number of ports than the second switch (Lou, see col.30, ln.20-25).” Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention to have a greater number of ports in a first switch taught by Lou into the VLANs of Shankar in order to implement different VLAN domains and to have backup ports in the first switch when the ports of the first switch are used as ingress ports.

Regarding claim 66, it is a claim corresponding to claim 4 and 6 and is therefore rejected for the similar reasons set forth in the rejection of claims 4 and 6.

Regarding claim 67, it is a claim corresponding to claim 4 and 7 and is therefore rejected for the similar reasons set forth in the rejection of claims 4 and 7.

Regarding claims 68-72, they are claims corresponding to claims 10-15, respectively and are therefore rejected for the similar reasons set forth in the rejection of the claims.

Regarding claim 73, it is a claim corresponding to claim 65 and is therefore rejected for the similar reasons set forth in the rejection of claim 65.

Regarding claims 74-80, they are claims corresponding to claims 66-72, respectively and are therefore rejected for the similar reasons set forth in the rejection of the claims.

Regarding claims 82 and 84, Shankar discloses, “wherein the two or more entities comprise a switch”, but lacks what Lou discloses, “the system further means for extending the number of ports of switch (col.30, ln.20-25).” Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention to have a means to extend the number of ports according to their needs in switch taught by Lou into the VLANs of Shankar in order to implement different VLAN domains and to have backup ports in the first switch.

Response to Arguments

8. Applicant's arguments with respect to claim have been considered but are moot in view of the new ground(s) of rejection. Please see the rejections in this Office Action for the added claim limitations.

Allowable Subject Matter

9. Claims 85-87 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jung Park whose telephone number is 571-272-8565. The examiner can normally be reached on Mon-Fri during 7:00-3:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edan Orgad can be reached on 571-272-7884. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you

have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Jung Park/
Examiner, Art Unit 2419

/Edan Orgad/
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